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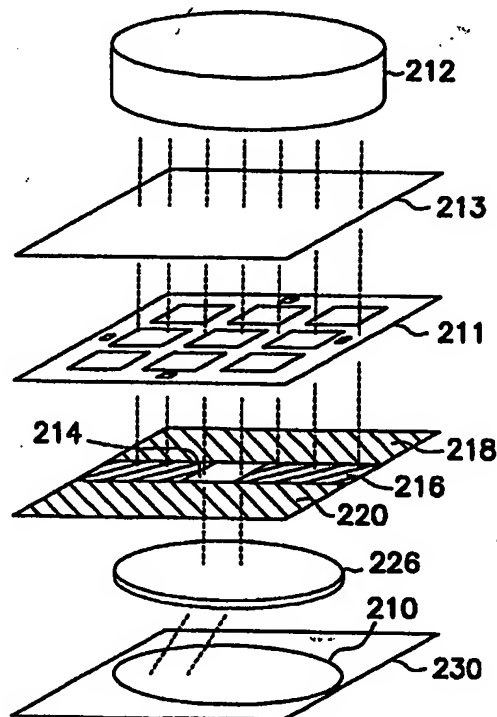
## INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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(21) International Application Number: <b>PCT/US98/17160</b> (22) International Filing Date: <b>19 August 1998 (19.08.98)</b> (30) Priority Data: <b>08/914,417</b> <b>19 August 1997 (19.08.97)</b> <b>US</b> (71) Applicant: <b>MICRON TECHNOLOGY, INC. [US/US]; 8000 South Federal Way, Boise, ID 83716-9632 (US).</b> (72) Inventor: <b>PIERRAT, Christophe; 9753 W. Preece, Boise, ID 83704 (US).</b> (74) Agent: <b>HOLLOWAY, Sheryl, S.; Schwegman, Lundberg, Woessner &amp; Kluth, P.O. Box 2938, Minneapolis, MN 55402 (US).</b>		(81) Designated States: <b>AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, HR, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</b>  <b>Published</b> <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: **MULTIPLE IMAGE RETICLE FOR FORMING LAYERS**

## (57) Abstract

A multi-image reticle used to form integrated circuitry comprises a two dimensional array of spaced images arranged in a matrix of controllably spaced rows and columns of images on a single reticle. No rotation of the reticle is required to expose various levels of circuitry on a semiconductor wafer. The wafer is held in a stepper device, which controllably positions the wafer under the desired image of the mask for exposure of a resist on the wafer. A movable aperture controls exposure through a selected image or mask pattern on the reticle. By controlling which image is used, and accurately positioning the wafer via the stepper, multiple images are accurately registered, leading to improvement in dimensions of circuitry and other structures formed on the wafer.



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## MULTIPLE IMAGE RETICLE FOR FORMING LAYERS

5

### Technical Field of the Invention

The present invention relates generally to optical lithographic techniques used in the formation of integrated circuits and structures on a wafer. In particular, the present invention relates to a reticle having multiple exposure  
10 patterns and its use.

### Background of the Invention

Lithographic methods use multiple images or masks to expose patterns in a resist layer on a semiconductor wafer for the formation of integrated circuits and structures such as processors, ASICS and Dynamic Random Access Memory  
15 (DRAM). As manufacturing requirements call for exposure of patterns with smaller and smaller dimensions, it is becoming necessary to employ techniques which permit enhancement of the current performance of the process of photolithography. Multiple successive steps of photolithography, film growth, deposition and implantation of impurities create a complete integrated circuit with  
20 many identical copies on the same wafer. Each copy is known as a die.

As integrated circuits have become smaller in dimensions, the photolithographic process requires more sophistication in alignment techniques and resolution. Presently, photo lithographic processes utilize an instrument referred to as a stepper which moves and aligns the wafer based on alignment marks on a  
25 reticle containing an image or mask such that desired patterns on the wafer are exposed based on the image. The reticle contains one or more images which may be referred to as levels because each image is used to form a level on the wafer. Light of a desired wavelength is either projected through or reflected by a selected image from the reticle to expose the substrate. Phase shifting methods,  
30 and electron beams, x-rays and ion beams are also used to pattern wafers.

Initially, each reticle contained only one image for forming one level. Reticles were becoming expensive to make due to the exacting conditions required to form smaller and smaller image lines. At the same time, complex integrated circuits required more and more levels and hence a high number of

reticles were required to form them. The cost of the reticles required to form the circuits was becoming great. This trend is continuing as chip densities continue to increase.

One proposed solution to this problem is described in U.S. Patent No. 4,758,863 entitled Multi-Image Reticle. Multiple images were formed on a reticle that was then rotated to expose the wafer using a different image for each level of an integrated circuit formed on the wafer. While this proposed solution reduced the need to keep changing reticles, it still introduced error into the image alignment process. First, each image had to be properly placed at different angles with respect to each other on the reticle. This introduced a rotational alignment error. Error was also introduced when a reticle was not perfectly centered. Rotation of the mask then produced a radial registration error. In addition, the angle of rotation of the mask holder introduced a further rotational alignment error. These errors made it difficult to properly align each reticle based on alignment images through the use of microscopes and other automatic alignment systems. To overcome rotational errors, a further degree of freedom than just movement in the x and y direction was required.

One further problem with this solution is that it left much space unused on the mask. Up to four images are shown on a reticle. There is wasted space, and a practical limit of about four square images which can be used. If more than four square images are used, they must be located further from the center of the reticle to fit within a slice of the reticle. This would further waste space on the reticle.

There is a need reduce the alignment error inherent in the use of multiple images on a reticle, and there is a further need to increase the number of images and hence reduce the cost of reticles.

#### Summary of the Invention

A multi-image reticle comprises a two dimensional array of spaced images or mask patterns arranged in a matrix of controllably spaced rows and columns on a single reticle. The images are aligned consistently in the same direction such that no rotation of the reticle is required to expose the levels on a wafer. The wafer is located on a stepper, which controllably positions the wafer under the

desired image of the mask for exposure of a resist on the wafer. In one embodiment, X and Y controlled opaque blades or shutters are used to define a movable aperture to allow exposure to occur only through a selected image on the reticle. In a further embodiment, a focussing device is moved to control  
5 which image is used. By controlling which image is used, and accurately positioning the wafer via the stepper, multiple images are accurately and repeatably registered, leading to improvement in dimensions of circuitry and other structures formed on the wafer.

In one embodiment, the images are designed for use with a phase shifting  
10 reflective and/or refractive mask. In this embodiment, radiation is reflected by each multi layer image to take advantage of interference patterns which are controlled to obtain desired exposure of the resist. Near the boundaries of exposed resist corresponding to the edge of the images on the reticle, the exposure received may be near zero. This can lead to undesired lines being  
15 "printed." To prevent the printing of such undesired lines, a second image on the reticle, either adjacent to the first, or placed anywhere else on the reticle is positioned to expose a second pattern over the first exposure to remove such lines prior to processing of the resist. Since no additional alignment errors are introduced, excellent registration with the previous exposure is obtained. Further  
20 images may also be aligned and exposed prior to processing the resist if desired.

Reticle costs are reduced because nine or more image patterns are located on the same reticle. Misregistration is reduced due to the ability of the stepper to position the target under the correct image using global x and y degrees of freedom without introducing errors through rotation of the reticle or having to  
25 load and accurately register a new mask. Optimal use of reticle space is made by use of an array of optimally laid out multi size rectangular images allowing a great reduction in the number of reticles and hence cost and time required to manufacture them. This can be a significant cost savings with respect to the manufacture of complex devices such as memory arrays, ASICs, processors and  
30 other integrated circuits.

The invention is particularly useful where multiple exposures are used prior to processing a resist to strip away desired areas. Since the level spacing is

tightly controlled, and no unload and load of a new mask is required, registration of the two exposures is extremely consistent. Many different types of lithography may be used, including photolithography using either reflective or refractive photomasks, electron beam lithography, x-ray lithography and ion beam

5 lithography to name a few.

#### Brief Description of the Drawings

Figure 1 is a plan view of one embodiment of a multi-image reticle.

Figure 2 is an elevational block diagram view illustrating the use of the multi-image reticle.

10 Figure 3 is a table of images on the reticle of Figure 1 used to form each layer on a semiconductor wafer.

#### Detailed Description of the Invention

In the following detailed description of the preferred embodiment, reference is made to the accompanying drawings which form a part hereof, and in  
15 which is shown by way of illustration specific preferred embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical and electrical changes may be made without departing from the scope of the  
20 present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

In the process of forming a pattern by use of photolithography, it is customary that a member used to pattern one integrated circuit on a  
25 semiconductor wafer is termed a reticle, and a member for exposing the entire wafer is termed a mask; or a member corresponding to an original sheet is termed a reticle, and a member obtained by duplicating such a reticle is termed a mask. In the present invention, a device for holding multiple such masks and reticles classified by such various definitions is referred to as a reticle for convenience.  
30 The terms image and mask pattern are used to refer to a structure on the reticle that is used to modify radiation such that it modifies a radiation sensitive material called a resist on a semiconductor wafer in a desired manner. It may do so by

reflection, refraction or a combination of both. The radiation may be in the any range of the electromagnetic spectrum suitable for modifying the resist. The modification of the radiation also comprises phase shifting methods to obtain suitable interference patterns.

5       With reference to Figure 1, a multi-image reticle 10 comprises a transparent substrate which is generally planar and essentially free of defects on the surfaces, as well as internally, and should have high optical transmission or reflection at a desired resist exposure wavelength. Several types of glasses have been used for making reticles, including: soda-lime glass, borosilicate glass, and  
10   quartz. However, quartz is the type of glass used in this embodiment. Other materials compatible with the resist process are acceptable, particularly when a material has favorable transmissivity characteristics when the wavelength of the exposure light source is less than 180 nm.

After the reticle 10 has been polished, cleaned and inspected, it is ready to  
15   be coated by reflective materials to form multiple integrated circuit mask patterns or images 112a, 112b, 112c, 112d, 112e, 112f, 112g, 112h, and 112i which are spaced in rows and columns in a rectangular array. There are nine such images shown in Figure 1. The nine images are arranged in three rows and three columns having substantially equal spacing between each image in each row and  
20   between each image in each column. It should be noted that the number of such images on the reticle may be varied to include fewer or thirty or more images depending on the physical limitations mandated by equipment and design rules for forming semiconductor circuitry. The spacing of such images may also be varied by the designer, but should be consistent with control parameters of a stepper  
25   described below. The reflective materials have refractive indices and absorption coefficients which determine a reflectivity and phase shift provided. In a phase shifting reflective photomask, radiation is reflected by the images such that constructive and destructive interference takes place favorably to form a highly resolved pattern on a desired surface. In a refractive or transmittive photo mask  
30   as described with reference to Figure 2, radiation is transmitted through the reticle to expose a photo resist in a desired pattern on a semiconductor wafer. It should be noted that reticles containing images suitable for many kinds of

lithographic processes, including photolithography using either reflective and refractive photomasks, electron beam lithography, x-ray lithography and ion beam lithography to name a few, may also be used without departing from the scope of the present invention.

5 A plurality of alignment images 114, 116, 118 and 120 are also provided on the periphery of reticle 110. These images are used in a known manner to provide for registration of the reticle and images projected on a wafer such that the images projected are properly aligned with previously formed structures on the wafer. They may be placed in various positions to ensure proper alignment of  
10 the reticle and registration of the images.

Each of the images in a reticle 211 comprise suitable patterns for forming circuitry on a suitably prepared substrate of a semiconductor wafer as shown at 210 in Figure 2 using well known lithography techniques employing a resist which is conventionally applied to the wafer as desired. The resist is exposed  
15 using radiation controlled by selected images on the reticle, then processed to remove the exposed areas which are processed using conventional film growth, deposition, implantation and other techniques. Then, the remainder of the resist is usually removed and then reapplied prior to the next exposure cycle.

A conventional controlled radiation source 212 such as a lamp, selectively  
20 projects radiation, first through a condenser 213, through the reticle 211 and then through an aperture 214 provided by conventional aperture blades 216, 218, 220 and 222. The aperture blades are movable as desired to cause the radiation from a single desired image on reticle 211 at any one time to pass. While shown in an exploded block diagram form, it is recognized that the aperture blades are much  
25 closer to the reticle 211 than shown. The radiation passing through the aperture is focussed by projection optics 226 onto the wafer 210. Wafer 210 is coupled to a conventional stepper 230 to provide exposure of a resist in a controlled manner. Wafer 210 comprises conventional semiconductor wafers of any size and material. In one embodiment, a silicon wafer of between 5 and 12 inches is used.

30 Since many identical circuits are formed on wafer 210, stepper 230 is used to step the radiation pattern through each of the separate circuits, referred to as die. When they are fully formed, each die will be cut and encapsulated to form an



integrated circuit chip. The stepper 230 is a very precise instrument which can repeatedly step from die to die once the initial image is properly registered. Since the reticle contains multiple images, it need only be aligned precisely once in a reticle holder of the stepper in order to be positioned correctly relative to the wafer. It is then used to help form multiple layers of circuitry. Thereafter, the moveable aperture 214 and stepper 230 are used to control which image is projected, and where it is projected. It is an easy matter to control the spacing of the images on the reticle when making the reticle to ensure that registration of images on the wafer is maintained by the stepper once initially registered.

10 Misregistration is reduced due to the ability of the stepper to position the target under the correct image using global x and y degrees of freedom, without introducing errors through rotation of the reticle or having to load and accurately register a new mask. Optimal use of reticle space is made by use of a rectangular array of rectangular images consistently aligned in the same direction allowing a

15 great reduction in the number of reticles and hence cost and time required to manufacture them. The blades 214, 216, 218, and 220 need only be moved back and forth to move the aperture to allow light to project onto the correct image. No rotation of the reticle is required. The reticle may also be moved in the x and y direction in order to position images to make use of desired lens 226

20 characteristics. The use of multiple images on a single reticle can be a significant cost savings with respect to the manufacture of complex devices such as memory arrays, ASICs, processors and other integrated circuits.

In a further embodiment, images may be of different sizes and shapes as shown in the reticle 211 of Figure 2. This permits optimal use of space on the

25 reticle by allowing placement of images as desired. Since images are usually rectangular in shape, their edges line up nicely with little space between them. This is highly contrasted with the prior art method requiring rotation of the reticle to use different images. Each such image must fit within a pie shape, which inherently leads to inefficient utilization of reticle space. Larger images must be

30 located further from the center of the reticle in order to fit within the pie shape. They still must line up with the circuit being formed when correctly rotated.

In one embodiment, each image on the reticle of the present invention is used to help form one level of circuitry or structure. Up to nine different levels may be formed using the reticle shown in Figure 1. With more images on the reticle, even higher numbers of levels may be formed. This provides a great savings in the cost of forming circuitry, as the cost of each reticle can be a significant part of the cost of manufacturing the circuitry. Some circuitry can require more than 20 different levels to form. By greatly reducing the number of reticles required, significant cost savings are obtained. It can also take significant time to form each reticle. The reduction in the number of reticles thus saves significant time.

One further benefit of the present invention is the ability to perform multiple exposures prior to processing the resist. This is very useful in embodiments which use phase shift based lithography. In such embodiments, radiation is reflected by each multi layer image to take advantage of interference patterns which are controlled to obtain desired exposure of the resist. Near the boundaries of exposed resist corresponding to the edge of the images on the reticle, the exposure received may be near zero. This can lead to undesired lines being "printed." To prevent the printing of such undesired lines, a second image on the reticle, either adjacent to the first, or placed anywhere else on the reticle is positioned to expose a second pattern over the first exposure to remove such lines prior to processing of the resist. Since no additional alignment errors are introduced, excellent registration with the previous exposure is obtained. Further images may also be aligned and exposed prior to processing the resist if desired. Figure 3 illustrates the use of multiple exposures using a nine image reticle to form six levels. The first level is exposed using both the first and second images prior to processing of the resist. The second level is exposed using the third and fourth images prior to processing the resist. The third and fourth levels are exposed using the fifth and sixth images respectively with the resist being processed each time. Level five also is exposed to two images, seven and eight, prior to resist processing, while level six is only exposed using image nine.

While the invention has been described with respect to particular embodiments, it will be recognized by those skilled in the art that other

embodiments may also be used with the present invention. The number of images per reticle, and their shape and spacing may be varied without departing from the scope of the present invention. Further, different frequencies of radiation may also be used with suitable resists.

What is claimed is:

1. A reticle for use in controllably exposing a wafer with desired patterns, comprising:
  - 5 a substrate;  
a plurality of spaced apart independent images provided on the substrate consistently aligned substantially in the same direction.
2. The reticle of claim 1 wherein the plurality of spaced apart images  
10 comprises substantially rectangular images arranged in rows and columns.
3. The reticle of claim 2 wherein the images are arranged in rows and columns.
- 15 4. The reticle of claim 2 wherein each image corresponds to a different level of circuitry to be formed on the wafer.
5. The reticle of claim 2 wherein at least two images correspond to one level of circuitry to be formed on the wafer.
- 20 6. A method of forming multiple levels of circuitry on a semiconductor wafer comprising the steps of:
  - aligning a multi-image reticle;
  - projecting radiation onto a first image of the reticle;
  - 25 modifying the radiation via the first image;
  - positioning an aperture between a light source and the wafer to pass light from a selected image;
  - focusing the radiation onto a selected portion of the wafer;
  - repeating the positioning, projecting, modifying and focusing steps for
  - 30 further images on the multi-image reticle without rotation of the reticle.

7. The method of claim 6 wherein the wafer is first coated with a resist prior to exposure to the radiation.
8. The method of claim 7 wherein the resist is processed following each exposure.
9. The method of claim 8 wherein a circuit layer is formed following processing of the resist.
10. The method of claim 9 wherein the remaining resist is removed following formation of the circuit layer.
11. The method of claim 10 wherein a further layer of resist is formed on the wafer following removal of the remaining resist.
12. The method of claim 11 wherein the resist comprises photo sensitive resist.
13. A method of forming circuitry on a semiconductor wafer comprising the steps of:
- coating the wafer with a radiation sensitive resist;
  - aligning a multi-image reticle;
  - projecting radiation onto a first image of the reticle;
  - modifying the radiation via the first image;
  - focusing the radiation onto a selected portion of the wafer;
  - projecting radiation onto a second image of the reticle;
  - modifying the radiation via the second image;
  - focusing the radiation onto the wafer to at least partially overlap the selected portion; and
  - processing the resist following exposure of the wafer by radiation modified by both the first and second images.

14. A process for imaging a semiconductor wafer in the production of integrated circuits, said process comprising the steps of:

providing a single multi-level reticle comprising a multiplicity of integrated circuit mask patterns, wherein said mask patterns are positioned in  
5 separate areas on said reticle;

providing a stepper device which is adapted to receive the multi-level reticle and which is further controllable to project light onto selected ones of the patterns;

inserting the reticle into the stepper device;

10 aligning the reticle;

projecting light onto one of the patterns to expose the wafer with a first pattern;

moving at least one of an aperture associated with the stepper and the reticle in only x and y directions;

15 projecting light onto a different one of the patterns as controlled by the relative positions of the reticle and aperture to expose the wafer with a second pattern in registration with the first pattern; and

employing growth techniques between at least some of the exposures to produce the desired integrated circuits on the wafer.

20

15. A reticle adapted for use in a photo lithographic system for causing multi-level images to be formed onto a substrate of a semiconductor wafer, the reticle comprising:

a plurality of distinct mask patterns positioned in separate areas on the  
25 reticle wherein the patterns are consistently aligned in the same direction to provide image registration on the substrate.

16. The reticle of claim 15 wherein the plurality of spaced apart mask patterns comprise substantially rectangular patterns arranged in rows and columns.

30

17. The reticle of claim 16 wherein the mask patterns are arranged in rows and columns having substantially equal spacing between each mask pattern in each row and between each mask pattern in each column.
- 5 18. The reticle of claim 16 wherein each mask pattern corresponds to a different level of circuitry to be formed on the wafer.
19. The reticle of claim 16 wherein at least two mask patterns correspond to one level of circuitry to be formed on the wafer; and
- 10 each one of said mask patterns correspond to various levels of circuitry to be formed on the substrate.
20. A multi-level reticle comprising a multiplicity of integrated circuit mask patterns, wherein said patterns are positioned in separate areas on said reticle,
- 15 wherein said reticle is adapted to be received in a stepper apparatus for projection of light through one of patterns on the reticle to project a mask pattern onto a substrate for forming an image, wherein at least one of the substrate and the reticle is adapted to be moved in the x and y direction relative to each other in a manner such that each of the mask patterns can be projected onto the substrate in
- 20 registration with the image, wherein the patterns are positioned in an array of rows and columns with substantially identical orientation of each pattern.
21. A multi-level reticle comprising a multiplicity of integrated circuit mask patterns, wherein said patterns are positioned in separate areas on said reticle,
- 25 wherein said reticle is adapted to be received in a stepper apparatus for reflection of radiation from one of patterns on the reticle to project a mask pattern via a focusing device onto a substrate for forming an image, wherein at least one of the substrate, the focusing device and the reticle is adapted to be moved relative to each other in a manner such that each of the mask patterns is projectable onto the
- 30 substrate in registration with the image, and wherein the patterns are positioned on the reticle with substantially identical orientation of each pattern.

22. The reticle of claim 21 wherein the plurality of spaced apart mask patterns comprise substantially rectangular patterns arranged in rows and columns.
23. The reticle of claim 21 wherein the mask patterns comprise 9 mask  
5 patterns arranged in three rows and three columns having substantially equal spacing between each mask pattern in each row and between each mask pattern in each column.
24. The reticle of claim 21 wherein each mask pattern corresponds to a  
10 different level of circuitry to be formed on the wafer.
25. The reticle of claim 21 wherein at least two mask patterns correspond to one level of circuitry to be formed on the wafer.



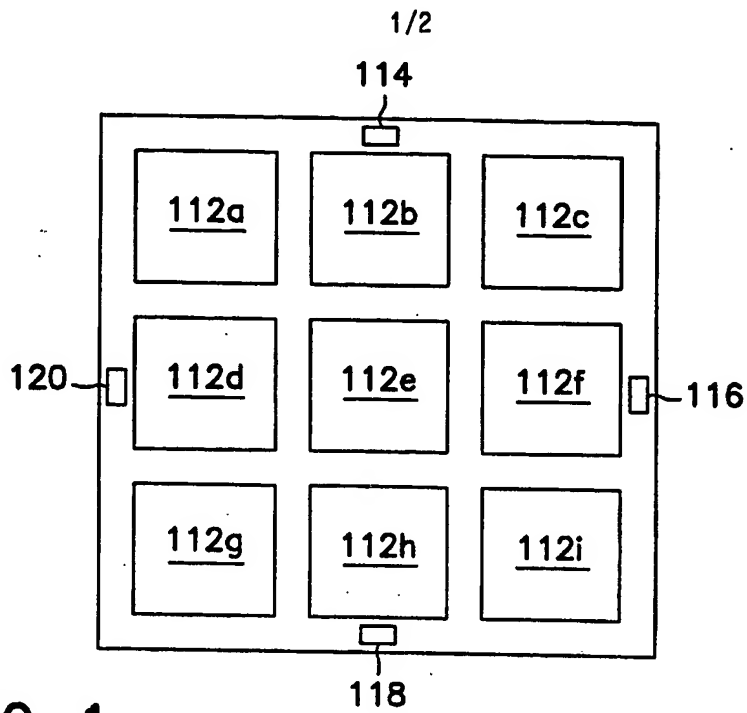


FIG. 1

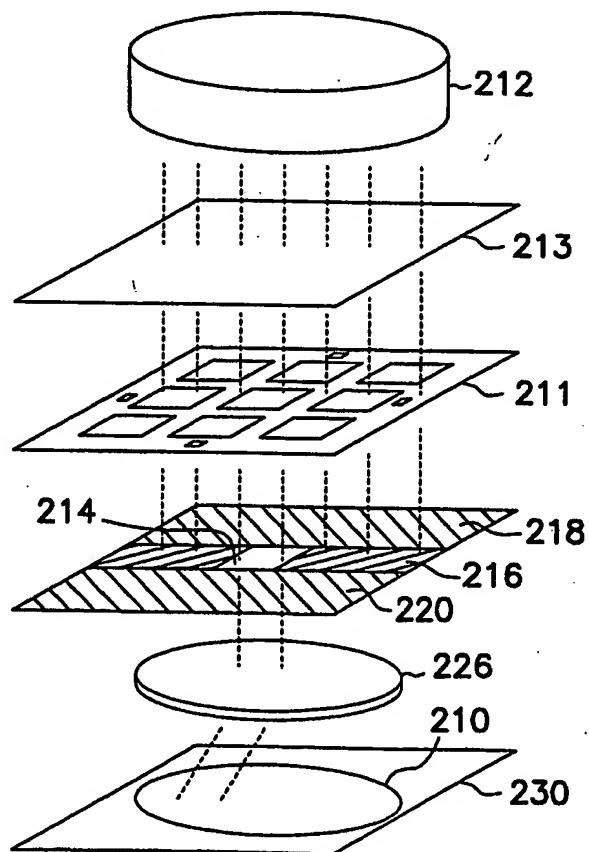


FIG. 2

LEVEL	EXPOSURE	IMAGE	PROCESS RESIST
1	Y	1	N
1	Y	2	Y
2	Y	3	N
2	Y	4	Y
3	Y	5	Y
4	Y	6	Y
5	Y	7	N
5	Y	8	Y
6	Y	9	Y

FIG. 3

# INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 98/17160

## A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 G03F1/14 G03F7/20

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 748 478 A (SUWA KYOICHI ET AL) 31 May 1988 see the whole document	1-20
X	GB 2 190 215 A (SMITHS INDUSTRIES PLC) 11 November 1987 see the whole document	1-3, 5, 15-17, 19
X	EP 0 518 783 A (FUJITSU LTD) 16 December 1992 see the whole document	1-20
X	PATENT ABSTRACTS OF JAPAN vol. 010, no. 084 (P-442), 3 April 1986 & JP 60 221757 A (HITACHI SEISAKUSHO KK), 6 November 1985 see abstract	1-3, 5, 15-17, 19



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PCT/US 98/17160

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 4748478 A	31-05-1988	JP 2593440 B	26-03-1997
		JP 62145730 A	29-06-1987
		DE 3643578 A	02-07-1987
GB 2190215 A	11-11-1987	DE 3714203 A	05-11-1987
		FR 2598233 A	06-11-1987
		US 4869998 A	26-09-1989
EP 0518783 A	16-12-1992	JP 2663063 B	15-10-1997
		JP 4364716 A	17-12-1992
		DE 69213111 D	02-10-1996
		DE 69213111 T	16-01-1997
		KR 9514064 B	20-11-1995
		US 5256881 A	26-10-1993